

FOLEY LARDNER
ATTORNEYS AT LAWWASHINGTON HARBOUR
3000 K STREET, N.W., SUITE 500
WASHINGTON, D.C. 20007-5143
TELEPHONE: 202.672.5300
FACSIMILE: 202.672.5399
WWW.FOLEYLARDNER.COM**FACSIMILE TRANSMISSION**Total # of Pages **2** (including this page)

TO:	PHONE #:	FAX #:
Examiner Kebede U.S. Patent and Trademark Office	703-306-4511	703-306-4511

From : Leon Radomsky
Sender's Direct Dial : 202.945.6090
Date : October 15, 2002
Client/Matter No : 035905-0104
User ID No : 2350

MESSAGE:

Application No.: 09/927,648

If there are any problems with this transmission or if you have not
received all of the pages, please call 202.672.5340.

Operator:	Time Sent:	Return Original To: Michelle T. Schwalbach
-----------	------------	---

CONFIDENTIALITY NOTICE: THE INFORMATION CONTAINED IN THIS FACSIMILE MESSAGE IS INTENDED ONLY FOR THE PERSONAL AND CONFIDENTIAL USE OF THE DESIGNATED RECIPIENTS NAMED ABOVE. THIS MESSAGE MAY BE AN ATTORNEY-CLIENT COMMUNICATION, AND AS SUCH IS PRIVILEGED AND CONFIDENTIAL. IF THE READER OF THIS MESSAGE IS NOT THE INTENDED RECIPIENT OR ANY AGENT RESPONSIBLE FOR DELIVERING IT TO THE INTENDED RECIPIENT, YOU ARE HEREBY NOTIFIED THAT YOU HAVE RECEIVED THIS DOCUMENT IN ERROR, AND THAT ANY REVIEW, DISSEMINATION, DISTRIBUTION OR COPYING OF THIS MESSAGE IS STRICTLY PROHIBITED. IF YOU HAVE RECEIVED THIS COMMUNICATION IN ERROR, PLEASE NOTIFY US IMMEDIATELY BY TELEPHONE AND RETURN THE ORIGINAL MESSAGE TO US BY MAIL. THANK YOU.

DO NOT ENTER / FOR DISCUSSION PURPOSES ONLY

- 1 I Pages 19-21 describe preferred generic concepts of a 3D array. Claims 99-120 and 456-481 are directed to this feature. *Fig. 35-36*
- 2 II Pages 22-49 describe the pillar device embodiment. Claims 1-12 are directed to this feature.
- 3 III Pages 23-43 are directed to pillar TFT EEPROMs, while pages 48-49 are directed to the diodes. Claims 64-98 and 13-63, respectively, are directed to these features.
- 4 IV Pages 49-73 are directed to self aligned TFTs. Claims 121-217 are directed to these features.
- 5 V Pages 74-86 are directed to rail stack TFTs. Claims 218-337 are directed to these features. *Fig 52*
- 6 VI Pages 86-97 are directed to a flash rail stack TFT memory. Claims 401-448 are directed to these features. *Fig 68-892*
- 7 VII Pages 97-106 are directed to a CMOS logic array. Claims 338-400 are directed to these features. *83-86*
- 8 VIII Pages 106-111 are directed to metal induced crystallization in a TFT. Claims 449-455 are directed to these features. *87-92*
- Fig 93-96*

<p><i>Generic Ideas</i></p> <hr/> <p>456, 467, 475</p> <p>3D - with CMP</p>	<p><i>Drivers in Substrate</i></p> <p>C-99 \Leftrightarrow Fig. 35</p> <hr/> <p>C-106-120 \Leftrightarrow</p> <p>Self aligned</p>
---	---

456-482

\odot ————— \odot